Remarks/Arguments

35 U.S.C. §103

Claims 1, 3-7, and 10, stand rejected under 35 U.S.C. §103(a) as being unpatentable over Valmiki et al. (U.S. Patent No. 6,636,222)("Valmiki"), in view of Terao et al. (U.S. Patent Publication No. 2001/0055011)("Terao").

The present invention, as recited by currently amended claim 1, describes an electronic apparatus comprising: a graphics memory storing a first and a second graphics object; an OSD processor generating a first digital stream representing the first graphics object; a pictures memory containing a picture and generating a second digital stream; a mixer able to mix the first digital stream and the second digital stream into a video signal; means for generating an overlap cue if an overlap is detected between the first and the second graphics objects; and means for converting the second graphics object into picture data if said overlap cue indicating said overlap between the first and the second graphics object is generated; and means for writing the picture data to the picture memory.

It is respectfully asserted that neither Valmiki nor Terao, alone or in combination, disclose "means for converting the second graphics object into picture data if said overlap cue indicating said overlap between the first and the second graphics object is generated," as described in currently amended claim 1.

Valmiki teaches a system where "a video and graphics system processes video data including both analog video, e.g., NTSC/PAL/SECAM/S-video, and digital video, e.g., MPEG-2 video in SDTV or HDTV format. The video and graphics system includes a video decoder, which is capable of concurrently decoding multiple SLICEs of MPEG-2 video data. The video decoder includes multiple row decoding engines for decoding the MPEG-2 video data. Each row decoding engine concurrently decodes two or more rows of the MPEG-2 video data. The row decoding engines have a pipelined architecture for concurrently decoding multiple rows of MPEG-2 video data. The video decoder may be integrated on an integrated circuit chip with other video and graphics system components such as transport processors for receiving one or more compressed data streams and for

extracting video data, and a video compositor for blending processed video data with graphics." (Valmiki Abstract)

The Office Action asserts that Valmiki discloses "the same structural properties of an electronic apparatus (see "Summary of the Invention") comprising: a graphics memory storing a first and a second graphics object (for "graphics memory" and "pictures memory" refer to column 6, lines 11-19 of Valmiki);an OSD processor generating a first digital stream representing the first graphics object; a pictures memory containing a picture and generating a second digital stream; a mixer able to mix the first digital stream and the second digital stream into a video signal; means for converting the second graphics object into picture data; means for writing the picture data to the picture memory (for "OSD processor" and "mixer" refer to column 5, lines 8-64 of Valmiki where graphics display system is OSD equivalent and video compositor is mixer equivalent. Furthermore, memory controller "reads and writes video graphics data to and from memory". Memory controller is also described as having "two substantially similar SDRAM controllers, one primarily for the CPU and the other primarily for the graphics display system, while either controller may be used for any and all of these functions")." (Office Action, pages 2-3)

A goal of the present invention is to work around the limitations of certain OSD processors, in particular the limitation that certain OSD processors cannot display two graphic objects that overlap, or in some cases, share the same lines of the screen. Therefore, the present invention discloses an apparatus that converts the second of two overlapped graphics into a stationary picture memory separate from the OSD path, which in turn is combined by a mixer with the OSD plane containing the first graphic. The end result is the display of the two overlapping graphics, despite the inability of the OSD processor to perform such display on its own. In contrast, Valmiki is not concerned with working around the limitations of OSD processors, but instead with rendering compressed video data within an allotted number of clock cycles. Valmiki discloses that its "video decoder includes multiple row decoding engines," but does not describe detection of overlaps or movement of an object from an OSD plane to a picture plane in response.

As such, Valmiki does not disclose means for converting a second graphics object into picture data if an overlap is detected between first and second graphics objects. Thus, it is respectfully submitted that Valmiki fails to disclose "means for converting the second graphics object into picture data if said overlap cue indicating said overlap between the first and the second graphics object is generated," as described in currently amended claim 1.

Terao teaches an invention whose goal is "to provide an information processor which, in case a component in which a moving picture is displayed is overlapped by another window, can apply display effect only to a region on which the moving picture is actually displayed." (Terao Abstract)

The Office Action asserts that Terao discloses "an overlap detector for detecting windows which overlap and prepares an overlap table accordingly as shown in Figures 5-8." (Office Action, page 3)

Terao does not disclose, nor does the Office Action assert it discloses, converting a second graphics object into picture data if an overlap is detected between first and second graphics objects. Therefore, Terao, like Valmiki, fails to disclose "means for converting the second graphics object into picture data if said overlap cue indicating said overlap between the first and the second graphics object is generated," as described in currently amended claim 1.

In view of the above remarks and amendments to the claims, it is respectfully submitted that there is no 35 USC 112 enabling disclosure provided by Valmiki or Terao, alone or in combination, that makes the present invention as claimed in currently amended claim 1 unpatentable. It is also respectfully submitted that independent claim 10 is allowable for at least the same reasons as currently amended claim 1. Since dependent claims 3-7 are dependent from allowable independent claim 1, it is submitted that they too are allowable for at least the same reasons claim 1 is allowable. Thus, it is further respectfully submitted that this rejection has been satisfied and should be withdrawn.

Having fully addressed the Examiner's rejections it is believed that, in view of the preceding amendments and remarks, this application stands in condition for allowance. Accordingly then, reconsideration and allowance are respectfully solicited. If, however, the Examiner is of the opinion that such action cannot be taken, the Examiner is invited to contact the applicant's representative at (609) 734-6804, so that a mutually convenient date and time for a telephonic interview may be scheduled.

No fee is believed due. However, if a fee is due, please charge the additional fee to Deposit Account 07-0832.

Respectfully submitted,

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